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EXAMINER	
PETRANEK, JACOB ANDREW	

ART UNIT	PAPER NUMBER
2183	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/561,454	ALBA PINTO ET AL.	
	Examiner	Art Unit	
	Jacob Petranek	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 January 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-8 and 10-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-8 and 10-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *1/6/2009* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-2, 4-8, and 10-12 are pending.

2. The office acknowledges the following papers:

Drawings, specification, claims, and arguments filed on 1/6/2009.

Withdrawn objection and rejections

3. The drawing objections are withdrawn due to amendment.

4. The specification objections are withdrawn due to amendment.

5. The claim objections are withdrawn due to amendment.

6. The 35 U.S.C. 112 second paragraph rejections for claims 1-8 and 10-11 have been withdrawn due to amendment.

Claim objections

7. Claim 12 is objected to for lacking a period at the end of the claim as required.

Drawing objections

8. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the limitations from claim 12 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended

replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

New Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 1-2, 4-8, and 10-11 are rejected under 35 U.S.C. §103(a) as being unpatentable over Sih et al. (U.S. 6,606,700), in view of Hennessy et al. ("Computer organization and design: the hardware/software interface"), in view of Sager et al. (U.S. 6,487,675).

11. As per claim 1:

Sih and Hennessy disclosed an instruction controlled data processing device, comprising:

an instruction issue unit that is configured to issue respective ones of instructions of program code in successive instruction cycles, the instructions including a first type of instruction and a second type of instruction (Sih: Figure 1 elements 104, 106, 118, and 120, column 3 lines 35-56)(MAC and Dual-MAC instructions execute on processing paths MAC1 and MAC2. Inherently, there is an instruction dispatch/issue unit to send these instructions to the execution units. It's obvious to one of ordinary skill in the art that instructions are issued each clock cycle and are of multiple instruction types.);

a clocking circuit that is configured to clock the instruction cycles (Hennessy: Figures 6.31-6.35)(The pipeline registers are inherently clocked by a circuit to control pipeline execution.);

a register file with a read port and a write port (Sih: Figure 1 element register file, column 3 lines 35-56)(The register file has read and write ports.);

plurality of functional units, each functional unit having a control input coupled to the issue unit (Sih: Figure 1 elements 104, 106, 118, and 120, column 3 lines 35-56)(Hennessy: Figure 6.30, page 469)(The combination results in the control signals shown in Hennessy being used to control the functional units of Sih.), an operand input coupled to the read port and a result output coupled to the write port (Sih: Figure 1 element register file, column 3 lines 35-56)(The inputs and outputs are coupled to the register files ports.);

a control unit coupled to the issue unit that is configured to route the result output of a first functional unit to the write port of the register file in response to instructions of the first type (Sih: Figure 1 elements 106 and 120)(Hennessy: Figure 6.28 and 6.29, page 469)(The combination uses the control signals of Hennessy to perform control operations in the processor of Sih. This allows for the execution results of the MAC2 processing path to write-back to the register file.), and to the operand input of a second functional unit during an instruction cycle in response to instructions of the second type (Sih: Figure 1 elements 106 and 120)(Hennessy: Figure 6.28 and 6.29, page 469)(The combination uses the control signals of Hennessy to perform control operations in the processor of Sih. This allows for the multiplication result to be sent to perform a Dual-MAC operation in the MAC1 processing path.)

The processor of Sih failed to show the inherent control signals and pipeline structure that are present to control the processor operations according to the decoded instructions. One of ordinary skill in the art would have been motivated by this lack of teaching by Sih to find Hennessy that discloses how a control unit controls the operations of a processor. Thus, one of ordinary skill in the art at the time of the invention would have been motivated to add the control signals and pipeline structure of Hennessy to the processor of Sih to show how all of the processor logic units are controlled during operation.

Sih and Hennessy failed to teach wherein the clock circuit is configured to vary a rate of clocking the instruction cycles in dependence upon whether a current segment of the program code includes one or more instructions of the second type.

However, Sager disclosed wherein the clock circuit is configured to vary a rate of clocking the instruction cycles in dependence upon whether a current segment of the program code includes one or more instructions of the second type (Sager: Figure 3 elements 220 and 225, column 4 lines 48-67 continued to column 5 lines 1-6)(Sih: Figure 1 element 116, column 3 lines 35-56)(The combination results in the MAC operations of Sih having a faster clock according to the intolerant sub-core and the Dual-MAC operations having a clock according to the tolerant sub-core.).

The advantage of dividing up the processor functions into a plurality of clock speeds allows for the slower speed functions to have a simplified design, which can lead to decreased chip space usage and power savings (Sager: Column 4 lines 3-20). One of ordinary skill in the art would have been motivated by this advantage to implement multiple clock speeds into the processor of Sih. Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to implement multiple clock speeds in the processor of Sih for the advantage of decreased chip space usage and power savings.

12. As per claim 2:

Sih, Hennessy, and Sager disclosed the processing device of claim 1, organized as a VLIW processor, wherein the issue unit includes a plurality of issue slots for issuing a VLIW instruction word (Sih: Figure 1 element 100)(Official notice is given that the processor of Sih can be organized as a VLIW processor. Thus, it's obvious to one of ordinary skill in the art that the processor of Sih is organized as a VLIW processor.), the register file having a plurality of sets of read and write ports (Sih: Figure 1 element

register file), the functional units or groups of functional units each coupled to a respective one of the issue slots and the sets of read and write ports (Sih: Figure 1 elements register file, 104, 106, 118, and 120)(The execution units are inherently coupled to the unit that issues instructions to them, as well as to the read and write ports.).

13. As per claim 4:

Sih, Hennessy, and Sager disclosed the processing device of claim 1, wherein the clock circuit includes a plurality of selectable clock rates, including a first clock rate that is sufficiently slow to accommodate a latency of instructions of the second type involved in producing a result from the second functional unit during execution of the instruction of the second type within the instruction cycle (Sager: Figure 3 elements 220 and 225, column 4 lines 48-67 continued to column 5 lines 1-6)(Sih: Figure 1 elements 118 and 120)(The combination results in the MAC instructions having a faster clock according to the intolerant sub-core and the Dual-MAC instructions having a clock according to the tolerant sub-core. The clocks are set according to the length of time required to execute each instruction.), and a second clock rate that is too fast to accommodate the latency of instructions of the second type in the instruction cycle, but accommodates latency of instructions of the first type (Sager: Figure 3 elements 220 and 225, column 4 lines 48-67 continued to column 5 lines 1-6)(Sih: Figure 1 elements 118 and 120)(The combination results in the MAC instructions having a faster clock according to the intolerant sub-core and the Dual-MAC instructions having a clock according to the tolerant sub-core. The clocks are set according to the length of time

required to execute each instruction. The intolerant core's clock cycle is set to execute the MAC instruction and not the Dual-MAC instruction.).

14. As per claim 5:

Sih, Hennessy, and Sager disclosed the processing device of claim 1, wherein the control unit is configured to selectively route the result output of a third functional unit to a further operand input of the second functional unit under control of the instruction of the second type (Sih: Figure 1 elements 146)(The MAC4 processing path is the third function unit and can selectively pass it's data to the second functional unit via the register file.).

15. As per claim 6:

Sih, Hennessy, and Sager disclosed the processing device of claim 5, wherein the program code includes a VLIW instruction that contains a command for the third functional unit and the instruction of the second type for issue in a same instruction cycle (Sih: Figure 1 element 100)(Official notice is given that the processor of Sih can be organized as a VLIW processor. Thus, it's obvious to one of ordinary skill in the art that the processor of Sih is organized as a VLIW processor. It's obvious to one of ordinary skill in the art that a Dual-MAC instruction and a MAC instruction can be scheduled in the same VLIW packet as long as there are no data dependencies.).

16. As per claim 7:

Sih, Hennessy, and Sager disclosed the processing device of claim 1, wherein the control unit is arranged to make the second functional unit respond to the instruction of the second type in an instruction execution cycle following an instruction execution

cycle in which the first functional unit responds to the instruction of the second type (Sih: Figure 1 elements 118 and 120)(It's obvious to one of ordinary skill in the art that Dual-MAC instruction can execute following a MAC instruction executing on the MAC2 processing path.).

17. As per claim 8:

Sih, Hennessy, and Sager disclosed the processing device of claim 7, wherein the result of the first functional unit is routed without intermediate latching from the first functional unit to the operand input of the second functional unit (Sih: Figure 1 element 116)(The output from the MAC2 processing path is sent to the MAC1 processing path.).

18. As per claim 10:

Sih and Hennessy disclosed a method of executing a processing task, comprising:

providing a group of functional units (Sih: Figure 1 elements 104, 106, 118, and 120, column 3 lines 35-56),

issuing successive instructions at an instruction cycle rate (Hennessy: Pages 466-468)(Instructions are dispatched after the register read stage.);

executing those of the instructions that are of a first type each with an individual one of the functional units during one instruction cycle (Sih: Figure 1 elements 106 and 120, column 3 lines 35-56)(Hennessy: Page 466)(The MAC instructions are executed in a clock cycle.),

executing an instructions that is of a second type with a first and a second one of the functional units in series during one clock cycle (Sih: Figure 1 elements 104, 116,

and 118, column 3 lines 35-56)(The Dual-MAC instructions are executed in series by multiplication followed by addition.);

routing a result of the first one of the functional units to an operand of the second one of the functional units in response to the instruction of the second type (Sih: Figure 1 element 116, column 3 lines 35-56)(The multiplication result of the MAC2 processing path is routed to the MAC1 processing path.).

The processor of Sih failed to show the inherent control signals and pipeline structure that are present to control the processor operations according to the decoded instructions. One of ordinary skill in the art would have been motivated by this lack of teaching by Sih to find Hennessy that discloses how a control unit controls the operations of a processor. Thus, one of ordinary skill in the art at the time of the invention would have been motivated to add the control signals and pipeline structure of Hennessy to the processor of Sih to show how all of the processor logic units are controlled during operation.

Sih and Hennessy failed to teach selecting the instruction cycle rate from at least a first and second rate, based on the type of instruction, the first rate being so slow that execution of instructions of a second type by a cascade of at least two of the functional units fits within an instruction cycle at the first rate, the second rate being so fast that only execution of instructions of the first type fits within the instruction cycle at the second rate, execution of instructions of the second type not fitting within one instruction cycle at the second rate.

However, Sager disclosed selecting the instruction cycle rate from at least a first and second rate, based on the type of instruction, the first rate being so slow that execution of instructions of a second type by a cascade of at least two of the functional units fits within an instruction cycle at the first rate (Sager: Figure 3 elements 220 and 225, column 4 lines 48-67 continued to column 5 lines 1-6)(Sih: Figure 1 elements 118 and 120)(The combination results in the MAC instructions having a faster clock according to the intolerant sub-core and the Dual-MAC instructions having a clock according to the tolerant sub-core. The clocks are set according to the length of time required to execute each instruction.), the second rate being so fast that only execution of instructions of the first type fits within the instruction cycle at the second rate, execution of instructions of the second type not fitting within one instruction cycle at the second rate (Sager: Figure 3 elements 220 and 225, column 4 lines 48-67 continued to column 5 lines 1-6)(Sih: Figure 1 elements 118 and 120)(The combination results in the MAC instructions having a faster clock according to the intolerant sub-core and the Dual-MAC instructions having a clock according to the tolerant sub-core. The clocks are set according to the length of time required to execute each instruction. The intolerant core's clock cycle is set to execute the MAC instruction and not the Dual-MAC instruction.).

The advantage of dividing up the processor functions into a plurality of clock speeds allows for the slower speed functions to have a simplified design, which can lead to decreased chip space usage and power savings (Sager: Column 4 lines 3-20). One of ordinary skill in the art would have been motivated by this advantage to

implement multiple clock speeds into the processor of Sih. Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to implement multiple clock speeds in the processor of Sih for the advantage of decreased chip space usage and power savings.

19. As per claim 11:

Sih, Hennessy, and Sager disclosed the method of claim 10, including:

issuing the successive instructions each as part of a VLIW instruction word that contains a plurality of instructions for respective further functional units (Sih: Figure 1 element 100)(Official notice is given that the processor of Sih can be organized as a VLIW processor. Thus, it's obvious to one of ordinary skill in the art that the processor of Sih is organized as a VLIW processor.);

including in the instruction word that contains the instruction of the second type a further instruction for a particular one of the further functional units (Sih: Figure 1 element 100)(Official notice is given that the processor of Sih can be organized as a VLIW processor. Thus, it's obvious to one of ordinary skill in the art that the processor of Sih is organized as a VLIW processor. It's obvious to one of ordinary skill in the art that a Dual-MAC instruction can be scheduled in a VLIW packet.);

routing a further result of the further instruction from the particular one of the further functional units to a further operand input of the second one of the functional units in response to the instruction of the second type (Sih: Figure 1 element 116, column 3 lines 35-56)(The execution data from the MAC2 processing path is routed to the MAC1 processing path.).

20. Claim 12 is rejected under 35 U.S.C. §103(a) as being unpatentable over Sih et al. (U.S. 6,606,700), in view of Hennessy et al. ("Computer organization and design: the hardware/software interface"), in view of Sager et al. (U.S. 6,487,675), further in view of Kim et al. (U.S. 2004,0225868)

21. As per claim 12:

Sih, Hennessy, and Sager disclosed the method of claim 10.

Sih, Hennessy, and Sager failed to teach including adapting the instructions used to execute the processing task to the selected instruction cycle rate, so that the instructions of the second type are used when the task is executed at the first rate and the instructions of the second type are replaced by instructions of the first type with corresponding effect when the task is executed at the second rate.

However, Kim disclosed including adapting the instructions used to execute the processing task to the selected instruction cycle rate, so that the instructions of the second type are used when the task is executed at the first rate and the instructions of the second type are replaced by instructions of the first type with corresponding effect when the task is executed at the second rate (Kim: Figure 4 element 412, paragraph 30)(The combination results in the instructions of Sih being able to be replaced at compile time to ensure optimal performance. Thus, Dual-MAC instructions executing in the latency tolerant execution core can be converted to MAC instructions to execute in the latency intolerant core when extra performance is needed.).

The advantage of replacing instructions in Sih with either low power or high performance instructions is that it allows for the program to either use less power executing a program or increase the performance of the program by running it faster (Kim: Paragraph 6). One of ordinary skill in the art would have been motivated by this advantage to implement the method of replacing instructions in Kim into the processor of Sih and Sager. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement the method of replacing instructions in Kim into the processor of Sih and Sager for the advantage of allowing for either lower power usage or increased performance while executing a program.

Response to Arguments

22. The arguments presented by Applicant in the response, received on 1/6/2009 are partially considered persuasive.

23. Applicant argues "Neither Rozenshein nor Hennessey, individually or collectively, teaches instructions of first and second types, wherein a rate of clocking instruction cycles is varied in dependence upon whether a current segment of program code includes one or more instructions of the second type, as claimed in amended claim 1, upon which claims 2 and 4-8 depend. Accordingly, the applicants respectfully request the Examiner's reconsideration and withdrawal of the rejection of claim 1-2 and 5-8 under 35 U.S.C. 103(a) over Rozenshein and Hennessey."

This argument is found to be persuasive for the following reason. The examiner agrees that these two references failed to teach the newly claimed limitation. However, a new ground of rejection has been given due to the amendment.

24. Applicant argues "The Office action acknowledges that Rozenshein fails to teach selecting an instruction cycle rate from a first and second rate, and asserts that Sager provides this teaching at column 4, line 48 - column 5, line 6). The applicants respectfully disagree with this assertion. Sager teaches partitioning a processor into a collection of high-speed latency-intolerant elements, and a collection of lower-speed latency-tolerant elements, and operating each of these partitions at different clock speeds. Sager does not teach selecting an instruction cycle rate for issuing instructions. Within Sagar's processor the two different clock speeds are always provided, all of the elements within the high-speed partition are operated using the high-speed clock, and all of the elements within the lower-speed partition are operated using the low-speed clock" for claim 10

This argument is not found to be persuasive for the following reason. The applicant's is generally correct in the assessment of Sager. However, a clock rate is selected based on the instruction to be executed. Thus, the latency intolerant clock rate is selected based on instructions being decoded and sent to that execution core. In addition, the latency tolerant clock rate is selected based on instructions being decoded and sent to that execution core. Thus, during instruction execution, the clock rate used to execute instructions varies dependent upon which type of instructions are decoded and sent to their corresponding execution cores.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jacob Petranek whose telephone number is 571-272-5988. The examiner can normally be reached on M-F 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Eddie P Chan/
Supervisory Patent Examiner, Art Unit 2183

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